(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 305 148 A1**

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(12) # EUROPEAN PATENT APPLICATION

(21) Application number: **88307805.7**

(22) Date of filing: **23.08.88**

(51) Int. Cl.[4]: **G 01 R 31/28**
G 01 R 31/04

(30) Priority: **26.08.87 US 89638**

(43) Date of publication of application:
01.03.89 Bulletin 89/09

(84) Designated Contracting States: **DE FR GB**

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(54) **Determining component orientation.**

(57) A system and method for unambiguously determining the orientation of a semiconductor component (48,50,52) in a circuit. The invention draws a predetermined biasing current from the signal node (74,80) of a circuit that is sufficient to forward bias protection (28) and/or parasitic (32) diodes that exist between the ground pin (62,64,66) and signal pin (46,70,72,76,78,82) of the semiconductor component (48,50,52). Hence, if all of the semiconductors coupled to a signal node are connected in proper orientation, a voltage of $-V_D$ will be detected on the signal node (74,80). A voltage of approximately two diode voltage drops is applied to the power node so that the protection (28) and/or parasitic (32) diodes of a semiconductor (48,50,52) placed in the circuit in reverse orientation will be forward biased to produce a voltage on the signal node (74,80) equal to approximately one diode voltage drop. Missing components and bent pins do not affect the results of the test performed by the present invention. Guarding techniques on the signal node are not required since impedances coupled to the signal node (74,80) are normally high enough to allow the protection (28) and/or parasitic (32) diodes to be forward biased by current supplied by the current source (84,86).

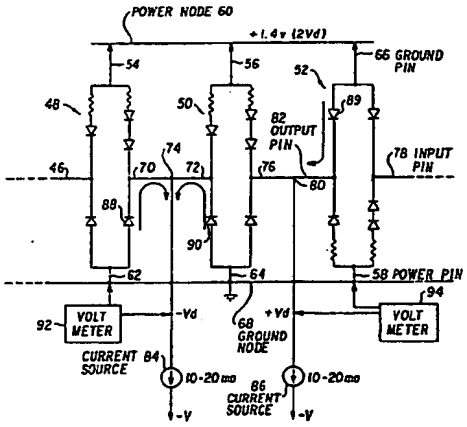

FIG. 4

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Description

DETERMINING COMPONENT ORIENTATION

Background of the Invention

1. Field of the Invention.

The present invention pertains generally to measuring and test devices and more particularly to manufacturing defect analyzers for testing digital components.

2. Description of the Background

Devices for testing printed circuit boards have typically fallen into three major categories. i.e., functional testers, in-circuit testers and manufacturing defect analyzers. Each of these three major categories of testers is briefly described below.

Functional testers comprise devices which have typically measured the output performance of a printed circuit board based on a series of input signals. Although functional testers provide an excellent way of testing the end desired performance of a particular board, they are usually incapable of determining the location of defects in the board, or components mounted on the board. As boards become larger, more complex, and costly, the chances of a defect occurring on a board, due to the many traces on the board, or one of the many components mounted thereon, increase greatly. Since functional tests merely indicate whether or not the board is operating properly and do not provide an indication of the location of a defect, the usefulness of functional testers as an overall test system is limited.

Because of the limitations of the functional testers in locating defects in boards, in-circuit test devices were developed. In-circuit test devices actually test individual components mounted on the board and test conductivity paths through the traces of the board by attaching a series of connector pins to various nodes on the circuit so that test signals can be applied to the components to determine operability. Algorithms have been developed to carefully limit the power which can be applied to components to prevent damage. Digital backdriving techniques have been integrated into the in-circuit testing scheme to allow both analog and digital components to be effectively tested in the in-circuit test devices. As circuit topologies have become more complex and the demand for faster in-circuit testers has grown, the in-circuit testing devices have become more and more expensive. This has resulted in a need for a less expensive device capable of testing simpler defects, such as open traces on a board or bent pins on a component.

Manufacturing defects analyzers were originally developed as inexpensive test devices for testing simple defects such as open circuits or short circuits on the printed circuit board. Since a high percentage of the faults on a board are produced by solder shorts between traces and other simple defects, manufacturing defect analyzers were developed to provide an inexpensive device for detecting a majority of these faults. Hence, manufacturing defects analyzers were able to fill a need for detecting simple defects on a printed circuit board without employing expensive in-circuit testing devices. Although analog testing techniques have been employed in some manufacturing defect analyzers, to date, very few have incorporated digital testing techniques because of the complexity and expense involved. Hence, manufacturing defect analyzers primarily remain as simple fault detection testers. Test Systems, Incorporated, located in Tempe, Arizona has designed several techniques for testing digital components in a simple and easy manner which can be employed in manufacturing defect analyzers. The Test System's circuit utilizes a voltage potential between the V_{CC} node and the signal node which is sufficient to forward bias a single diode junction but insufficient to forward bias two diode junctions. If the IC is inserted in reversed orientation, a large amount of current will flow from the VCC node to the input/output node (signal node) indicating that the IC has been inserted in reverse orientation. However, parallel conductive paths must be carefully guarded to ensure that false readings are not obtained from the test system. The guarding techniques required by the Test Systems, Incorporated device can often times be somewhat complex and difficult to implement. Hence, a need exists for a simple method of unambiguously determining whether an IC has been placed in the circuit in proper orientation.

Summary of the Invention

The present invention overcomes the disadvantages and limitations of the prior art by providing a system for unambiguously determining the orientation of a semiconductor component in a circuit. This is accomplished by providing a predetermined voltage on a power node of the circuit that is equal to approximately two diode junction voltage transitions. Additionally, a current sufficient to forward bias a single diode junction is drawn from a signal node so that a voltage equal to one diode junction voltage transition is produced by current flowing from the ground node through a diode junction coupled between the ground node and the signal connector. The advantages of the present invention are that it unambiguously identifies nodes connected to IC'S that have been placed in the circuit in reverse orientation. A substantial voltage difference is produced at the signal node for reverse oriented IC'S to clearly identify failing nodes. Additionally, bent pins or missing parts do not affect the test.

Only reversed IC'S will produce a voltage variation at the signal node. Additionally, unlike prior art devices, no guarding is needed for parallel conductive paths, especially conductive paths coupled to the signal node since a current is drawn from the signal node sufficient to forward bias diode junctions existing between the signal node and ground. The elimination of the necessity for guarding against parallel conductive paths greatly simplifies the implementation of the system.

Brief Description of the Drawings

An illustrative and presently preferred embodiment of the invention is shown in the accompanying drawings, wherein:

Figure 1 comprises an overall schematic view of the test system of the present invention.

Figure 2 discloses a typical schematic partial circuit diagram comprising a device under test.

Figure 3 schematically illustrates one possible circuit topology for the devices under test.

Figure 4 is a schematic illustration of an equivalent circuit showing the devices under test in the circuit topology illustrated in Figure 3.

Detailed Description of the Invention

Figure 1 is a schematic illustration showing the manner in which the present invention can be implemented in a test system. The printed circuit board 10 which is under test has a plurality of components 12 which are connected to the printed circuit board 10. Conductors 14 provide conductive traces between the various components 12. Testbed 16 has a plurality of connector pins 18 which are aligned to connect to various nodes of conductors 14 that are to be tested by the test system of the present invention. The connector pins 18 are coupled to a series of conductors 20, which are in turn, connected to test system 22. Test system 22 comprises a programmable computer or state logic device that is connected to the necessary drivers for generating currents and voltages, and the necessary detectors, comparators and other circuitry needed to perform the test functions of the present invention. The test system processes the information and displays results on display 24. Typically, failed nodes are compared with the conductivity information which is supplied to test system 22 to indicate specific IC'S which have been placed in the circuit in reverse orientation.

Figure 2 is a schematic illustration of a typical semiconductor circuit that comprises a device under test (DUT) that is being analyzed to determine if the DUT has been placed in the circuit in reverse orientation. Typically, the pin layout of the semiconductor is such that the ground pin and power pin of the semiconductor are on corresponding positions on opposite sides of the semiconductor. Hence, if the semiconductor is placed in the circuit in reverse orientation, the ground pin will be connected to the power node of the circuit while the power pin will be connected to the ground node of the circuit. Some symmetry of the semiconductor circuit provides a way of detecting if the IC has been placed in the circuit in reverse orientation.

Referring to Figure 2, input 26 is coupled to ground through a protection diode 28 which comprises a discrete component designed in the semiconductor circuit. In a similar manner, output 30 is coupled to ground with a parasitic diode 32 that is produced between the substrate and the output as a result of the manufacturing process. The base/emitter junction of transistor 34 provides a single diode junction between power pin (V_{CC}) 36 and input 26 that is connected in series with resistor 38. Similarly, resistor 40 is connected in series with the base/emitter junction of transistor 42, which is in turn connected in series with the base/emitter junction of transistor 44 between power pin 36 and output 30. The equivalent circuit for the device of Figure 2 is more fully set forth in Figure 4.

Figure 3 is a schematic illustration disclosing the manner in which a number of integrated circuits may be connected in series in a circuit topology on a printed circuit board 10. Although Figure 3 illustrates one manner in which a plurality of integrated circuits such as illustrated in Figure 2, may be connected, many other topologies may exist including fan-out nodes (Bus topologies) which are equally applicable for use with the present invention. As shown in Figure 3, input 46 of IC 48 can be coupled to other components or other integrated circuits within the circuit topology. IC's 48, 50 and 52 have power pins 54, 56 and 58, respectively, that are coupled to power nodes 60. Similarly, ground pins 62, 64 and 66 of IC'S 48, 50 and 52, respectively, are connected to ground nodes 68. As shown in Figure 3, output 70 of IC 48 is connected to input 72 of IC 50 at a signal node 74 of the circuit. Similarly, output 76 of IC 50 is connected to input 78 of IC 52 at signal node 80 of the circuit. Output 82 of IC 52 may be connected to one or more additional IC'S or other components of the circuit.

Figure 4 is a schematic diagram illustrating the equivalent circuit of Figure 2 for IC 48, IC 50 and IC 52 connected in the circuit topology illustrated in Figure 3 with the exception that semiconductor 52 is connected to the circuit in reverse orientation. The test system of the present invention utilizes a signal source 84 which draws a bias current of approximately 10 to 20 milliamps which is sufficient to forward bias diode junctions 88 and 90 which exist between the ground pin 62 and output pin 70 of integrated circuit 48 and the ground pin 64 and input pin 72 of integrated circuit 50. Diode junction 88 comprises a parasitic diode while diode junction 90 comprises a protection diode. The current which is drawn through the diodes 88 and 90 from signal node 74 produces a single diode junction voltage drop ($-V_D$) which is measured by voltmeter 92. Simultaneously, a voltage of approximately 1.4 volts is applied to power node 60 which is equal to approximately two diode voltage drops ($2V_D$). The voltage on power node 60 is insufficient to forward

bias the diodes of semiconductors 48 or 50 between power node 60 and signal node 74 because of the resistance which is in series in the signal paths between power node 60 and signal node 74. Hence, a measurement of minus one diode voltage drop ($-V_D$) by voltmeter 92 provides an indication that both semiconductors 48 and 50, coupled to signal node 74, are connected to the circuit in proper orientation. Of course, any number of semiconductors, such as semiconductors 48 and 50 can be coupled to a single signal node, such as signal node 74, without degrading the performance of the present invention. Additionally, as can be readily seen from the circuit illustrated in Figure 4, either semiconductor 48 or 50 could be missing from the circuit and the device of the present invention would still operate equally as well. Consequently, missing components do not degrade the performance of the present invention.

Semiconductors placed in the circuit in reverse orientation are detected in a slightly different manner. Referring to semiconductor 52 of Figure 4, the voltage applied to power node 60 is approximately two diode voltage drops, i.e., approximately 1.4 volts. Because semiconductor 52 is in reverse orientation, a diode junction 89 is coupled between the ground pin 66 and output pin 82 of semiconductor 52. As a result, diode junction 89 is forward biased by the voltage applied to power node 60. The voltage applied to power node 60 comprising two diode voltage drops ($+2V_D$) is used as a matter of convenience. Of course any voltage level sufficient to forward bias a single diode junction when the IC is placed in the circuit in reverse orientation is needed at power node 60, provided that the voltage level at power node 60 is less than that required to forward bias the diodes between power node 60 and any signal node when a semiconductor is placed in the circuit in proper orientation. Since diode junction 89 is forward biased, the voltage on power node 60 appears on signal node 80. This results in a single diode junction voltage drop across protection diode 89 so that a voltage level of $+V_D$ is detected at signal node 80 by voltmeter 94. Consequently, if any semiconductor component, such as semiconductor component 52, is placed in the circuit in reverse orientation, a voltage of $+V_D$ will be detected at signal node 80, rather than a voltage of $-V_D$ at a signal node such as signal node 74 to which all semiconductors are connected in proper orientation. A comparison of the connectivity charts and the failing nodes provides an indication of which IC'S within the circuit have been placed in the circuit in reverse orientation.

Again, if either semiconductor component 50 or 52 were missing from the circuit, the performance of the device of the present invention would not be degraded since only semiconductor components which are placed in the circuit in reverse orientation cause a $+V_D$ voltage reading at the signal node. This comprises a significant advantage over prior art devices that are affected by bent pins and missing components.

Consequently, the present invention provides a simple and inexpensive device that can be used to supplement manufacturing defect analyzers to determine if a semiconductor component has been placed in a circuit in reverse orientation. These results are obtained in an unambiguous manner and are not affected by missing components or bent pins. Guarding techniques are not necessary on the signal nodes since a current is being drawn from the signal node to forward bias the protection and parasitic diodes of properly oriented semiconductors. Impedances that are coupled to the signal node are normally great enough to prevent sufficient sinking of current from the signal node that would prevent forward biasing of these diodes. The elimination of the necessity for guarding, as required in prior art devices, greatly simplifies the implementation of the present invention.

Claims

1. A method of determining the orientation of a semiconductor component (48, 50, 52) which is coupled in a circuit to a signal node (74, 80) and a power node (60), comprising the steps of: applying a first voltage level to the power node (60) which is less than the voltage level necessary to forward bias a first diode junction or junctions of the semiconductor component (48, 50, 52) which is or are coupled between the power node (60) and the signal node (74, 80) when the semiconductor component (48, 50, 52) is correctly oriented in the circuit but greater than the voltage]eve] necessary to forward bias a second diode junction or junctions of the said semiconductor component which is or are coupled between the power node (60) and the signal node (74, 80) when the semiconductor component (48, 50, 52) is connected in circuit in an orientation opposite the said correct orientation; drawing a current from the said signal node (74, 80) which is sufficient to forward bias the said second diode junction or junctions of the semiconductor component (48, 50, 52); and detecting the potential difference between the signal node (74, 80) and the ground node (68) whereby to determine whether the said potential difference has a first value to indicate that the semiconductor component (48, 50, 52) is correctly oriented in the circuit, or whether the said potential difference has a second value to indicate that the semiconductor component (48, 50, 52) is coupled in circuit in the reverse orientation.

2. A method according to Claim 1 for determining if one of a plurality of semiconductor components is connected in reverse orientation in a circuit, characterised in that the said current is drawn from a plurality of respective signal nodes (74, 80) associated with respective pairs or groups of semiconductor components (48, 50, 52).

3. Apparatus for determining the orientation of a semiconductor component (48, 50, 52) connected in a circuit having at least one signal node (74, 80), at least one power node (60) and at least one ground node (68), the semiconductor component having at least one first diode junction coupled between the power node (60) and the signal node (74, 80) when

the semiconductor component is connected in the correct orientation, and at least one second diode junction (88, 89, 90) coupled between the signal node (74, 80) and the ground node (68) when the semiconductor component is connected in the correct orientation and between the power node (60) and the signal node (74, 80) when the semiconductor component is connected in reverse orientation, characterised in that it comprises voltage supply means for applying a predetermined supply voltage to the power node (60) which is not sufficient to forward bias the said first diode junction or junctions of the semiconductor component when the latter is connected in correct orientation in the circuit but sufficient to forward bias the second diode junction or junctions when the semiconductor component is connected in circuit in reverse orientation; current supply means (84, 86) for providing a predetermined bias current to the signal node (74, 80) sufficient to forward bias the said second diode junction or junctions when the said semiconductor component (48, 50, 52) is connected in circuit in proper orientation, and means (92, 94) for detecting the potential difference between the signal node (74, 80) and the ground node (68) whereby to determine if the semiconductor component (48, 50, 52) is connected in correct or reverse orientation.

4. Apparatus as claimed in Claim 3, characterised in that the said means (92, 94) for detecting the potential difference is at least one voltmeter.

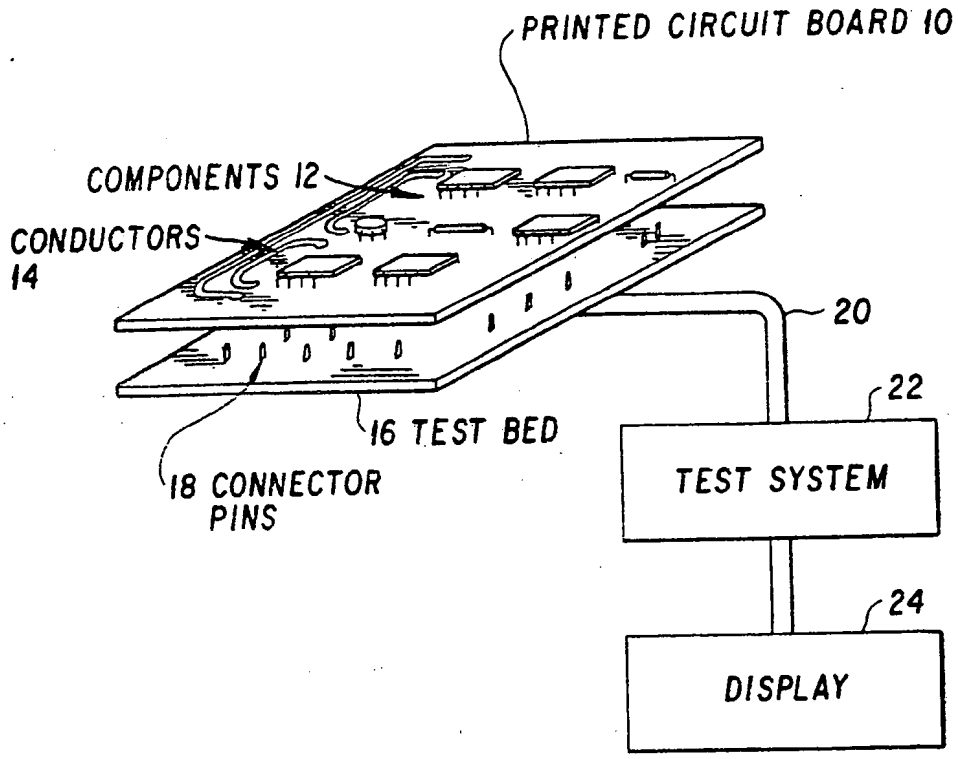

FIG. 1

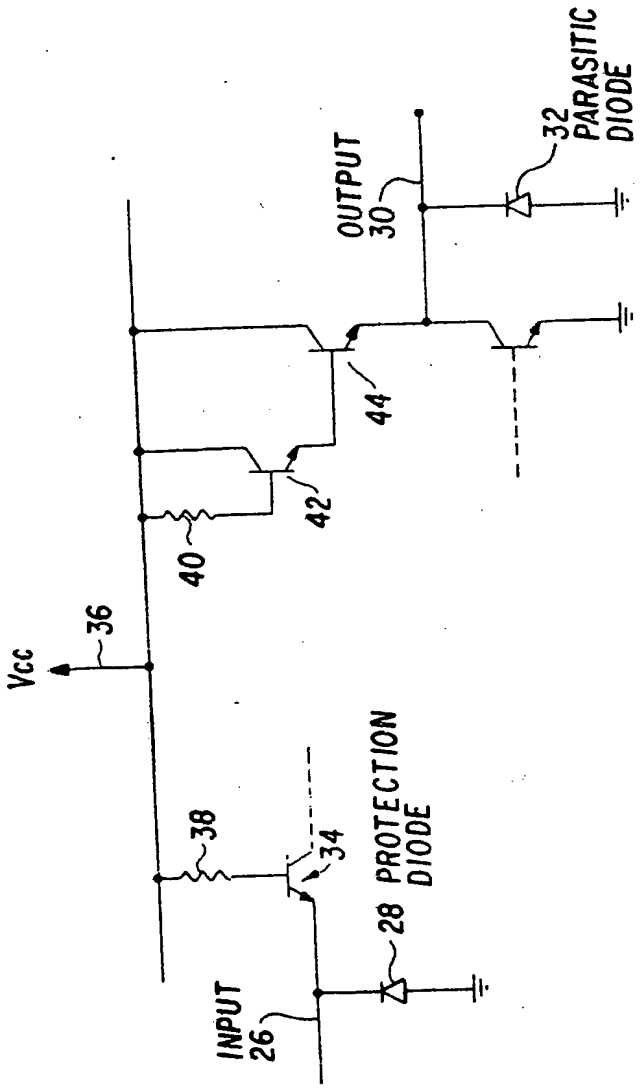

FIG. 2
(PRIOR ART)

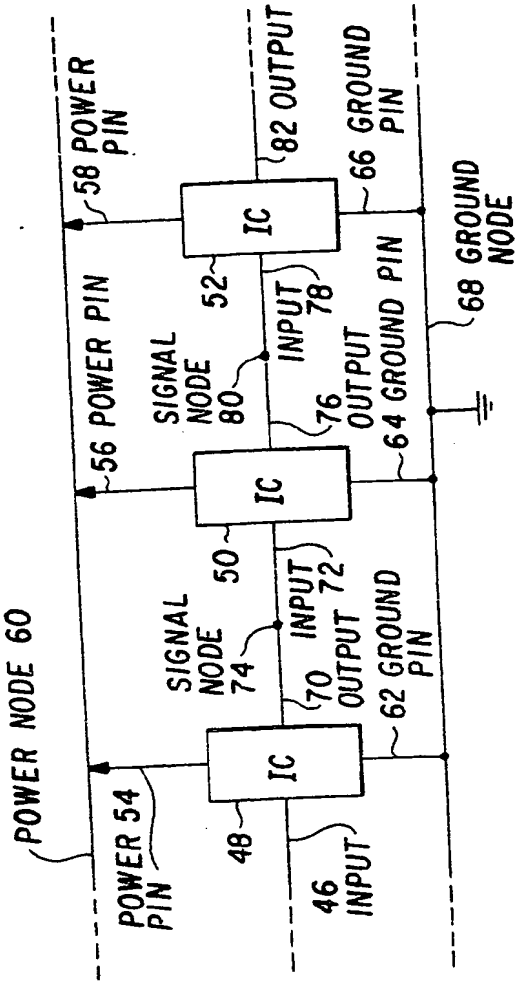

FIG. 3

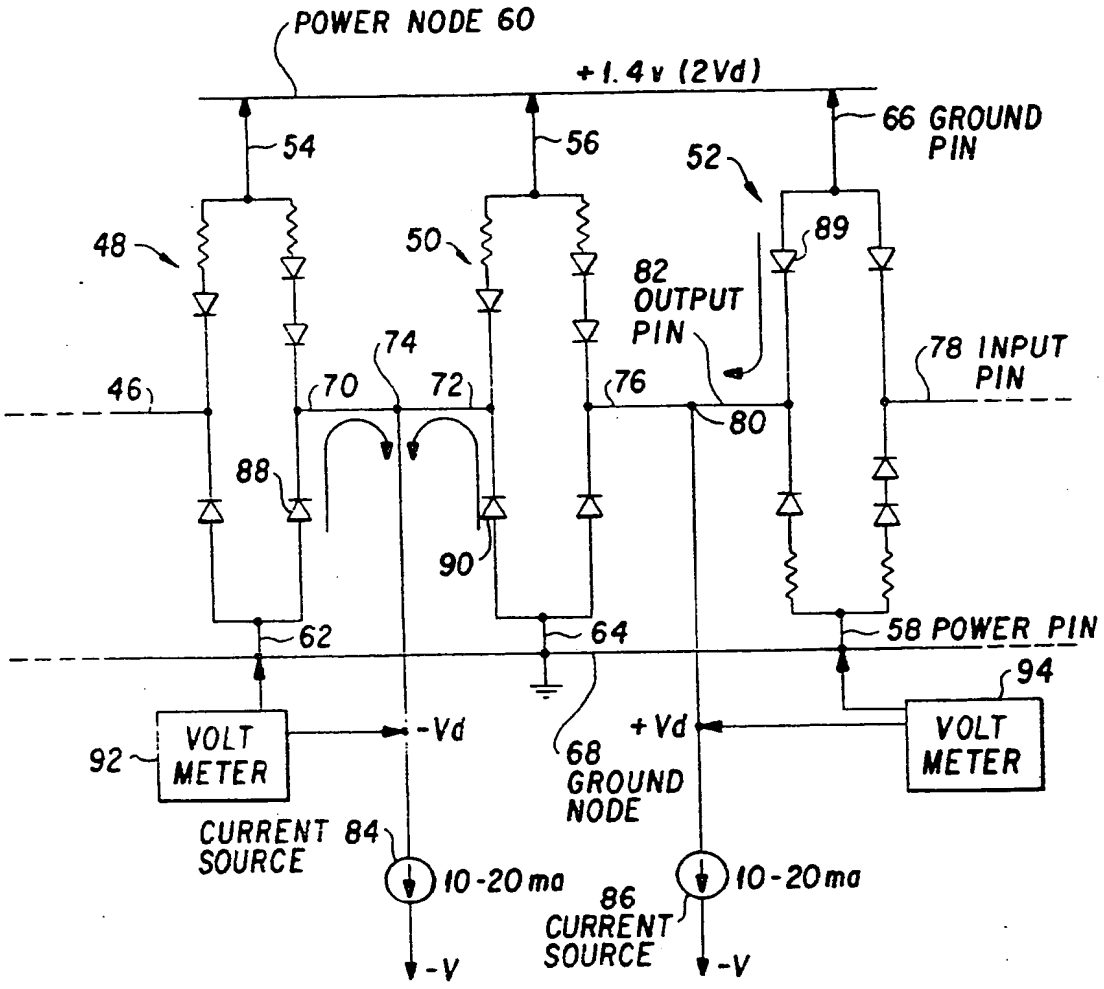

FIG. 4

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 88 30 7805

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.4)
X	GB-A-2 167 196 (MEMBRAIN) * Whole document *	1,2	G 01 R 31/28 G 01 R 31/04
A		3	
A	GB-A-1 376 595 (GENERAL ELECTRIC CO.) * Page 2, lines 109-116; claims 1,3 *	1-4	
A	GB-A-1 512 950 (PLESSEY) * Page 1, lines 34-76,85-88; figure 2 *	1-3	
A	PATENT ABSTRACTS OF JAPAN, vol. 6, no. 147 (E-123)[1025], 6th August 1982; & JP-A-57 69 756 (FUJITSU K.K.) 28-04-1982 * Abstract *	1,3	

TECHNICAL FIELDS SEARCHED (Int. Cl.4)

G 01 R
H 05 K
H 01 L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	24-11-1988	WIEMANN L.

CATEGORY OF CITED DOCUMENTS

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